REMARKS

Claims 2-6 and 8-14 are all the claims pending in the Application. By this Amendment, Applicant amends claims 2-4, 8-10 and 13 solely for the purpose of improved readability and to correct minor, basic elements. As such, Applicant respectfully submits that these amendments do not narrow the scope of the claims and do not raise any Festo implications.

Formal Matters

Applicant thanks the Examiner for accepting the Corrected Drawings filed April 1, 2003.

Applicant notes that a Notice of Improper Request for Continued Examination (RCE), mailed May 2, 2003, states that the RCE was not accompanied by a submission as required by 37 C.F.R. § 1.114. The Notice states that the Continued Prosecution Application (CPA) filed on April 21, 2003 was treated as an RCE because the CPA was filed in an application that was filed on or after May 29, 2000.

This Notice was erroneous, since the present Application was filed before May 29, 2000, as the cover page of the Notice itself acknowledges, noting a filing date of July 6, 1999. Further, the CPA requested entry of the Amendment filed April 1, 2003, which had not been entered. Therefore the CPA was properly filed.

On August 18, 2003, Applicant's representative contacted the Examiner to clarify this issue for the record, and the Examiner explained that the Notice was sent by a legal instrument specialist at the Patent Office, not the Examiner, and that the Notice should be ignored. The

Examiner explained that in any event, the present outstanding non-final Office Action (Paper No. 14) restarts the period available to the Applicant for responding to Paper No. 14.

Objections

I. The Examiner objected to the Specification, lines 2-4, page 4, and lines 15-17, page 6, as described in the Amendment filed April 1, 2003, because of the "by the computer" language. Please see below Applicant's traversal of the rejection of claims 3-6 and 9-12 under 35 U.S.C. § 112, First Paragraph. Accordingly, this objection should be withdrawn.

II. Claim Objections. The Examiner objected to claims 4 and 10 as containing the term $T_{connected\_fresh}$ and therefore being inconsistent with the term $T_{connect\_fresh}$ used in the equation. Claims 4 and 10 have been corrected to remove this inconsistency. The objection should now be withdrawn. This correction is not a narrowing amendment. No estoppel is created.

Rejection of Claims 3-6 and 9-12 under 35 U.S.C. § 112

Claims 3-6 and 9-12 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. This rejection is traversed.

The Examiner alleges that a person of ordinary skill in the art would not have known how two logic blocks as recited in the claims would have been connected to each other, whether by wire or by some intervening computer connected between them, since the Specification states

that "[t]he block-to-block delay time $T_{connect\_aged}$ is delay time of a signal passing between said two logic blocks connected to each other by a computer." (Specification, Page 4, underline added.) Therefore, the Examiner states that without undue experimentation it is unclear how one skilled in the art could make and/or use the invention, since the calculation of the delay time introduced by the computer has not been disclosed in the Specification.

In making this rejection, the Examiner seems to set forth the written description requirement of 35 U.S.C. §112, First Paragraph, by stating that the rejected claims fail "to reasonably convey...that the inventor(s)...had possession of the claimed invention" (Paper No. 14, Page 3). However, the Examiner seems to base his argument, at least in part, on the enablement requirement "without undue experimentation, it is unclear how one skilled in the art may make and/or use the invention" (Paper No. 14, Page 4). Applicant assumes that the Examiner intended to make a "written description" rejection.

Applicant respectfully submits that based on Applicant's disclosure as a whole, one of ordinary skill would have readily understood that Applicant was in intellectual possession of the invention as claimed. First, as the title and the first paragraph of the Specification (page 1) make clear, the present invention deals with designing a semiconductor integrated circuit and in particular, with a method of verifying the reliability of the semiconductor integrated circuit. Paragraph two of the Specification states that a problem generally to be addressed by the present invention involves a circuit of a semiconductor integrated circuit, and the logic blocks that comprise a circuit of a semiconductor integrated circuit. Thus, given the context provided by the first two paragraphs alone, it is clear that an aspect of the invention is concerned with logic

blocks that are associated with a circuit of a semiconductor chip. Therefore, it is respectfully submitted that a person of ordinary skill would have understood that Applicant was in possession of the subject-matter concerning the connection of logic blocks of a semiconductor integrated circuit.

Further, the Specification explains that according to an aspect of Applicant's invention, a logic level circuit as organized such that it is comprised of logic blocks. "In general, a logic level circuit is divided into a plurality of logic blocks which may be considered as a minimum unit of the logic level circuit. In this event, it is necessary to acquire information concerning inner transistors for the calculation at every one of the logic blocks." (Specification, page 9, first full paragraph.) Thus, one skilled in the art would have readily understood that the logic blocks comprise a logic level circuit of a semiconductor integrated circuit. Therefore, it is respectfully submitted that one skilled in the art would have readily understood that Applicant was in possession of the claimed subject-matter.

More generally, the simulation discussed is delay time in a computer environment. Accordingly, for the simulations discussed, the expression "[t]he block-to-block delay time $T_{connect\_aged}$ is delay time of a signal passing between said two logic blocks connected to each other by a computer" is not incorrect, and should be understood as stating that the two logic blocks are connected to each other "by a computer" meaning "for," or "as part of," "a computer" application or environment.

Rejection of Claims 13 and 14 under 35 U.S.C. § 112

Claims 13 and 14 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. This rejection is traversed.

The Examiner alleges that in claim 13, with respect to the recitation "wherein in the first calculation means, the plurality of V_C values includes exclusively a V_C value of a transistor connected directly to an input pin of the logic block and a V_C value of a transistor connected directly to an output pin of the logic block" the addition of the words "includes exclusively" in the previous Amendment is new matter unsupported by Applicant's original disclosure.

Applicant's disclosure states that "it has also been found that Tr211 and Tr221 connected directly to the input and output pin tend to seriously influence these effects.... Consequently, it is very effective to calculate the effect of hot electron [the hot-carrier effect] only in connection with ... transistor Tr211 and Tr221." (Specification, page 9, underline added.) Thus, the Specification clearly states that hot-carrier effect for only the transistors connected to the input pin and the output pin is one possible way of providing the solutions disclosed.

In addition, several equations, including by way of illustration, not by way of limitation, Equations (5) and (6) for the delay time of the pin-to-pin path make use only of the transistors connected to the input and output pins. (Specification, page 11.) Therefore, Applicant respectfully submits that the "includes exclusively" language was fully supported by Applicant's

originally filed disclosure and that one skilled in the art would have readily understood that Applicant was in possession of the invention as claimed in claim 13.

Claim 14 depends from independent claim 13 and was rejected under 35 U.S.C. § 112, First Paragraph, only because of its dependence from a rejected claim. Therefore, claim 14 should now be allowed.

Rejection of Claims 4, 6, 10, and 12 under 35 U.S.C. § 112

Claims 4, 6, 10, and 12 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. This rejection is traversed.

The Examiner alleges that λ is defined as "a delay time" and based on that definition it is unclear to one of ordinary skill in the art without undue experimentation, why the value λ is not ½ because in the middle stage the input changes from high level to low level with zero delay time. Similarly, expressions (33) and (34) with respect to four-stage logic block are unclear (see page 5 of the Office Action). For clarification purposes only, claims 4 and 10 have been amended to recite "delay time degradations".

Applicant notes that as known in the art, N-channel transistors are seriously effected by the hot carrier effect (for example, *see* page 8, line 27 to page 9, line 7 of the Specification). This hot carrier effect causes aging of the N-channel transistors, which in turn impacts the delay time.

For example, in case of a three-stage logic, as shown in Figure 6, if input changes from the low level to high level (causing hot carrier effect, which in turn causes aging), both of the N-channel transistors at the input and output stages work. The aging of these working N-channel transistors influences the delay time. Consequently, $\lambda_{in} = \lambda_{out} = 1/3$, as shown in the expression (31), wherein denominator 3 symbolizes the number of stages. On the contrary, if the input to the inverter changes from high level to low level, then no damage to the inverter is caused by the hot carrier effect. As a result, there is no delay as shown in the expression (32), $\lambda_{in} = \lambda_{out} = 0$.

In case of a four-stage logic block, when the input changes from the low level to the high level, the input stage transistor works and influences the delay time, whereas the output stage transistor does not work as such it obviously does not influence the delay time. Therefore, expression (33) shows $\lambda_{in} = ¼$ and $\lambda_{out} = 0$. On the other hand, when input changes from high level to low level, only the output transistor influences the delay time, as such expression (34) shows $\lambda_{in} = 0$ and $\lambda_{out} = ¼$.

As such, the relationship between the delay time and hot carrier damage is disclosed. In addition, claims 4 and 10, as now amended, recite "ratios of delay time degradations occurred at the input stage and output stage to whole delay time". Claims 6 and 12 were rejected only because of their dependence on claims 4 and 10. Therefore, Applicant respectfully submits that it is now proper and appropriate for the Examiner to withdraw this rejection of claims 4, 6, 10 and 12.

Rejection of Claims 2-3, 5, 8-9, 11, 13, and 14 under 35 U.S.C. § 103

Claims 2-3, 5, 8-9, 11, 13, and 14 are rejected under 35 U.S.C. § 103(a) as being obvious over Iwanishi, et al., (U.S. Patent No. 6,047,247), in view of Fang, et al., (U.S. Patent No. 6,278,964). This rejection is traversed.

Independent claim 2 requires, *inter alia*, calculating a numerical value V_B from a plurality of values V_C comprising only a first V_C value of a transistor connected directly to an input pin of the logic block and a second V_C value of a transistor connected directly to an output pin of the logic block. Independent claims 3 and 5 require, *inter alia*, calculating variations of signal delay times, based on V_C values comprising exclusively a transistor property of a transistor connected directly to the input pin and a transistor property of a transistor connected directly to the output pin. Further, independent claim 8 requires, *inter alia*, calculating the V_B from a plurality of numerical values V_C, wherein the plurality of V_C values comprises exclusively a V_C value of a transistor connected directly to an input pin and another V_C value of a transistor connected directly to an output pin. Independent claims 9 and 11 require, *inter alia*, calculating variations of signal delay times caused by aging based on transistor property values only for transistors inside the logic block connected directly to one of the input pin and the output pin of the logic blocks. Finally, independent claim 13 requires, *inter alia*, calculating value V_B, a property of a logic block, based on a plurality of numerical values V_C, wherein the plurality of V_C values includes exclusively a V_C value of a transistor connected directly to an input pin of the logic block and a V_C value of a transistor connected directly to an output pin of the logic block.

The Examiner acknowledges that Iwanishi does not disclose or suggest a V_C value representing a transistor property. However, the Examiner alleges that Iwanishi discloses calculating a cell property based on "circuit information," and that Fang discloses a hot-carrier effect calculation based on circuit information including device parameters of all elements of a circuit. The Examiner further alleges that if a cell comprised only a single inverter, the inverter would then be connected directly to an input pin of the cell.

First, neither Iwanishi nor Fang discloses or suggests a cell comprising only a single inverter. The Examiner has not cited any such disclosure or suggestion. In fact, a cell would typically consist of a number of transistors to make the cell useful in processing or representing a meaningful unit of binary information. Therefore, Iwanishi and Fang do not disclose or suggest calculating a numerical value V_B from a plurality of values V_C comprising only a first V_C value of a transistor connected directly to an input pin of the logic block and a second V_C value of a transistor connected directly to an output pin of the logic block, as *inter alia* required by claim 2, nor calculating variations of signal delay times, based on V_C values comprising exclusively a transistor property of a transistor connected directly to the input pin and a transistor property of a transistor connected directly to the output pin, as, *inter alia,* required by claims 3 and 5. Further, Iwanishi and Fang do not disclose or suggest calculating the V_B from a plurality of numerical values V_C, wherein the plurality of V_C values comprises exclusively a V_C value of a transistor connected directly to an input pin and another V_C value of a transistor connected directly to an output pin, as, *inter alia,* required by claim 8, nor calculating variations of signal delay times caused by aging based on transistor property values only for transistors inside the logic block

connected directly to one of the input pin and the output pin of the logic blocks, as *inter alia*, required by independent claims 9 and 11. Finally, Iwanishi and Fang do not disclose or suggest calculating value V_B, a property of a logic block, based on a plurality of numerical values V_C, wherein the plurality of V_C values includes exclusively a V_C value of a transistor connected directly to an input pin of the logic block and a V_C value of a transistor connected directly to an output pin of the logic block, as *inter alia*, required by independent claim 13.

Further, as discussed in the previous Amendment, there would have been no suggestion or motivation for combining Iwanishi and Fang. The Examiner alleges that the motivation would have been that Fang discloses in detail the circuit information. However, the Examiner does not explain why, without impermissible hindsight reconstruction, there would have been motivation to select from Fang any particular types of circuit information and combining them into Iwanishi to arrive at Applicant's invention.

Claim 14 depends from independent claim 13 and thus incorporates all the novel and nonobvious recitations thereof. Therefore, claim 14 is patentably distinguishable over the prior art for at least the reasons that claim 14 is patentably distinguishable over the prior art.

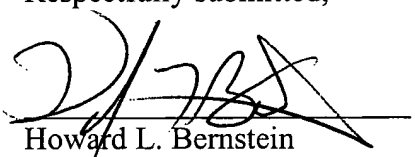
Conclusion

In view of the foregoing remarks, reconsideration and allowance of this Application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the

Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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